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PS

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/440,595	11/15/99	MAJID N	PHA-23843

MM92/0214

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EXAMINER	
PAREKH, N	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary

Application No.	Applicant(s)
09/440,595	Majid et al
Examiner	**Group Art Unit**
Nitin Par kh	2811

☒ Responsive to communication(s) filed on *Nov 15, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-8* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-8* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al (US Pat. 6130458) in view of the admitted prior art (APA- Japanese Pat. 6-169057A).

Regarding claim 1, Takagi et al disclose a multichip hybrid integrate circuit (IC)/module for high power applications comprising:

-a power semiconductor chip and (200 in Fig. 12A and B) and a control semiconductor chip (100 in Fig. 12A and B) mounted on an electrically conductive substrate connected to ground potential (81 in Fig. 12B) where the power semiconductor chip comprises a silicon-on-insulator device and the control semiconductor chip comprises a semiconductor device having a substrate connected to ground potential, and

- the power and control semiconductor chips are directly mounted on the electrically conductive substrate without the use of a separate electrical insulation layer (Fig. 12B)

(Fig. 12A and B; Fig. 15; Col. 11, line 30-Col. 12, line 57).

Takagi et al fail to specify the electrically conductive substrate connected to ground potential as being a heat sink substrate. The APA teaches using a multichip module with the chips mounted on a conventional metal heat sink/substrate. The cited reference (Hill- US Pat. 6028348) teaches using a heat sink substrate for a multichip power module (Fig, 3; Col. 2, line 66) for high power applications. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate an electrically conductive heat sink substrate connected to ground potential to achieve improved electrical and thermal performance using the APA's heat sink substrate in Takagi et al's multichip module as cited in claim 1.

Regarding claim 2, Takagi et al disclose the control semiconductor chip comprising CMOS or any other configurations comprising BICMOS, bipolar, n-MOS, etc. (Col. 13, line 64).

Claims 3 and 4 are rejected as explained above for claims 2 and 1.

Claim 5 is rejected as explained above for claim 1.

Claim 6 is rejected as explained above for claim 1.

Regarding claim 7, Takagi et al in view of the APA fail to specify the conductive/metal heat sink comprising copper metal. However, it is conventional in the chip packaging and interconnection technology art to use heat sink/metal substrates made of the metals such as copper, aluminum, etc. to improve heat dissipation for the module. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the conductive heat sink comprising copper metal to achieve improved electrical and thermal performance in Takagi et al's multichip module in view of the APA as cited in claim 7.

Claim 8 is rejected as explained above for claim 1.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

02-07-01

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER